An Active Learning / Teamwork Approach to Implementing an Integrated Circuit Design Cycle in an Advanced Hardware Description Language Course

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Abstract -- *The design of digital Application Specific Integrated Circuits (ASICs) has recently shifted from schematic entry toward the use of hardware description languages such as VHDL or Verilog. Powerful design tools are required to perform the design synthesis, simulation, and verification of these chips prior to fabrication. Most courses in VHDL or Verilog focus on the details of the language rather than the process and techniques required by industry in creating an actual chip. This paper describes an approach currently being used for an advanced VHDL course which attempts to have students learn not only the hardware description language, but also the design tools and process required to produce an actual working ASIC. In addition to discussing the learning techniques used, this paper will also describe handling issues such as uneven contribution efforts and individual assessment.*

The course is based on an active learning and teamwork approach to completing the design. Use of the design tools takes place at the beginning of the course, after which everyone should understand the fundamental processes of synthesis and simulation. Active learning methodologies will be used to strengthen the knowledge of VHDL as well as the procedures required for the design tools. Two teams of students are then formed, one for design and one for simulation/verification. The design team will concentrate on writing and synthesizing VHDL code which will meet the requirements of the ASIC, and the simulation team will be tasked with writing VHDL code which will be used to verify the chip meets the requirements prior to fabrication. The activities and progress of both teams will be discussed at joint meetings held each week. Due to a limited class size the instructor acts as a manager of each team as well as the entire project.

An upper level course in hardware description languages (HDL's) has been taught at Kansas State University, and traditionally the course has focused on the language syntax for the majority of a semester. Those who design with HDL's realize that more than syntax is required when designing a chip. Knowledge of the tools used to synthesize and verify the HDL design is inevitable due to variations in how each tool vendor implements the language. The complexities of the tools vary widely as some tools assume the user wants little control over logic synthesis while others give the designer virtually unlimited control and correspondingly a high level of complexity. This course has recently evolved to include a large amount of effort spent having the students learn to use a fairly complex set of synthesis and verification tools while completing a variety of projects resulting in actual circuits to be tested. Currently the course is undergoing a trial revision replacing some of the individual projects with a larger design project which the entire class will work on in a teamwork approach. VHDL was chosen as the primary HDL to be used during the semester.

The first eight weeks of the semester deal with learning VHDL and the basics of the synthesis and simulation tools. Various projects are implemented during this period, with the later projects concentrating on synthesis for FPGA architectures and implementing the designs on FPGA evaluation boards. Various techniques are used to enhance the learning during this period, including class discussions of VHDL code examples, laboratory classroom sessions, and the exchange of ideals, questions, and answers through a course email discussion group.

The second half of the semester is devoted primarily to achieving a system design using a team approach. Earlier in the semester the class discussed various project ideas, and collectively they decided to design a communications network between various FPGA boards, each of which would control a VGA display and receive input from a keyboard. The class discusses issues regarding this project during normal class time as well an additional one-hour meeting each week. Thus far the class has divided the design into four subsystems, and the interface for each subsystem has also been specified.

Both design and verification concepts are being emphasized throughout the semester, so each subsystem has assigned both a design and simulation team consisting of two to three members each. Each member is on both a design and verification team so they continue to get experience with both aspects. Although the instructor attempts to guide all teams, a leader has also been appointed for each team to oversee its progress. A tentative schedule has also been developed for this project which includes design reviews, target completion dates, implementation, testing, and revision opportunities. A formal set of documentation is required at the end of the semester.