A New eLearning System Integrating A Top-down eLearning and New Virtual Remote Laboratory Environments for Logic Circuit Design

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Abstract - A new distance learning system, integrating a top-down design support system and a multi-user/multi-test-bed remote laboratory system for digital circuit hardware design and implementation course, is realized. The proposed system employs the hardware description language (VerilogHDL) for the design database and FPGAs for design implementation test-beds. Students using this remote laboratory system at remote sites can perform actual hardware experiments in parallel. It realized a remote multi-user time-sharing hardware experiment system. It has achieved seamless remotes and actual hardware laboratories, which resolve conflicts among users, when many users request the same services at the same time. The top-down design support system guides students to complete projects. The course material database is organized in the form of a design-module-cell hierarchy tree, where each design-module-cell contains a sample circuit design, described in VerilogHDL. The use of XML wrapped VerilogHDL descriptions and specially extended XML vocabularies contributed to share designed modules among students and teachers as well across the Internet via the Web. The prototype of the distance learning system, integrating both the digital circuit design support system using top-down approach and the multi-user remote laboratory system for running experiment of digital circuit, has been developed. It has achieved an effective and efficient distance learning system.

Index Terms – Remote Laboratory, Job Management system, FPGA, VerilogHDL, Top-down Learning.

INTRODUCTION

This paper describes a new eLearning system combining a digital circuit design learning support system and a remote multi-user and time-sharing hardware experiment system.

A new learning support system adopted the top-down approach for digital circuits design, namely Top-Down eLearning System (TDeLS) [1] as digital circuit design education support system. TDeLS has been designed for learners to perform self-learning effectively. Using this system, learners can keep focusing on their primary interests to achieve their goals successfully, with minimum teachers' interventions or advice. The goal of the eLearning is to design the courseware within the Semantic Web environment [2]. The top-down method is employed for the design of this courseware. Furthermore the cellular data model [3] is adopted in order to ensure the consistency and to maintain the conformance among the learning contents data. It contains a database system based on the top-down technique [1]. The circuit modules are described by making use of Hardware Description Languages.

In a modern logic circuit design, the use of HDLs is becoming very popular. They contribute to reduce design effort and design time. It also makes it possible to share designed sub-circuit logic modules among learners and teachers. Without the help of such an eLearning system as we propose, it would be very difficult to keep the learners’ interests and motivations to lead them to the final goal. Many learners would be dropped out before reaching the final goal. The design support system traverses the design hierarchy tree to find out a suitable design sample module description, by making use of both depth-first and breadth-first search algorithms, according to students’ skill levels and learning histories.

Furthermore, a prototype of a new remote laboratory system for digital circuit experiments [4], has been developed. Hardware experimental environment is usually treated as an exclusive resource, for single user usage. However, the actual test run time is rather short and most of the time is wasted leaving those precious resources idle. This new remote laboratory system therefore employs a time-sharing fashion to make learners at remote sites perform actual experiments using actual hardware equipments and tools concurrently. Job Management System, named Condor [5], has been employed for the experimental environment allocations.

Authors already developed Top-down education System based on Cellular Models [1][6], which contributed to increase in efficiency of logic circuit study. In order to promote understanding of logic circuit design, authors realized the remote laboratory environment where logic circuit experiments can be conducted [7]. Furthermore, the effort was concentrated on the Web-based remote laboratory implementations [7][4]. In order to achieve more stable and
flexible experiment services for multiple users, the remote laboratory system adopted the available Condor job scheduler [5] and the prototype was re-organized[8][9].

Most existing learning and experiment systems are rather isolated each other. However, it is important that the learning system and the experiment system are tightly coupled. The proposed system integrated the top-down eLearning and the time-sharing multi-user remote laboratories. Thereby, the usefulness of the system to a user is demonstrated.

**BACKGROUND AND RELATED WORKS**

I. Distance Learning

A new top-down eLearning tool, which can efficiently retrieve suitable learning materials for designing circuit modules according to the learner’s skill levels, has been developed. It can dynamically navigate the design module hierarchy tree and recommend an appropriate circuit design description to assist the learner to achieve the learning goal effectively.

We took advantage of the top-down learning methods to enhance the learner’s design process. The top-down learning maintains learner's willingness to learn and improves the efficiency to achieve the final target. It shows the way to the final target clearly, and offers the optimized courseware to reach the goal. Recently, the importance of the curriculum organization, especially in the computer science education field, based on the top-down method, is recognized. The educational curriculum based on the top-down method is employed by several domestic and foreign universities and showed its effectiveness [10].

II. Hardware Experiment Environment

One of the emerging areas is the natural science field, where a number of design-and-experiment runs using actual equipments are inevitable. Although, there are many existing virtual remote laboratory environments in the field, most such systems are employing so-called “the Client-Server architecture”. However, applying simple Client-Server system for the scientific experiments has the following disadvantages: They can not, 1) perform actual experiments at the same time, 2) obtain actual measured data, and 3) utilize actual measurement equipments [11].

For natural scientific experiments such as computer design and implementation laboratory, it becomes very important to make use of actual hardware, to give actual input data, and to observe actual experiments. The existing client-server based remote laboratories cannot fulfill these requirements. In order to overcome these shortcomings, the author proposes the new virtual remote laboratory environment, which realizes an efficient sharing of test equipments and supports actual experiments runs/measurements concurrently.

The authors focused on the Web-based remote laboratory approach [4]. Once such a courseware has been implemented, the remote laboratories can take full advantages of new technologies, such as server-side technology, rich-client technology and the job manager. One of the distinguishing features of the proposed Web based experimental environment is its efficient remote-sharing capability of actual laboratory equipments. This remote laboratory system allows efficient sharing of the experiment platforms including target FPGA boards, real logic analyzers or real pattern generators.

In the past, the experiment platform including target FPGA board, logic analyzer and pattern generator were exclusively occupied by single user for a long period of time, once the user had started remote experiments. As these measurement equipments were so expensive that it became prohibitive to install sufficient number of equipments. The authors observed the usage of these test benches and addressed that the actual usage of the test bench was rather short comparing with other tasks, such as preparation, compilation and post-analysis. So, number of remote laboratory environments could efficiently share an actual test equipment, in a time division fashion. As the modern logic analyzers and pattern generators are offering PC-based measurement environments, the control software for these PC-based equipments can also be run on client PCs decoupled from actual measurement equipments. The job manager is employed for the Web based remote laboratory system, in order to perform the conflict-resolution among equipment usages, job-submissions and job-allocations.

**FIGURE 1**

**INTEGRATED SYSTEM OVERVIEW.**
II. Top-down eLearning System

The top-down approach is suitable to apply for the hardware logic design course where the learning goal is clear. Students are required to obtain logic circuit skills, to design and implement large scale logic circuits, such as 16 bit CPU. A data model, a data structure, and search algorithms play an important role in finding out learning contents according to the top-down approach.

- **Cell Data models**: The cell data models are based on the hierarchy of the abstract concepts, they include the characteristics of existing various data models. The data models are expressed by the composition of cell and pre-cell [3], as shown in the Figure 2. An ordered set of pre-cells is called a cell. A concept of the boundary is adopted in the cell theory, where a pre-cell is also called a boundary. It has connection information with other cells in this boundary.

- **Cell Data Structure**: The Figure 2 shows a connected situation of a pre-cell and a cell. Cell Pn-1 and pre-cell Pn-1 of cell Fn are connected.

**TABLE I**

<table>
<thead>
<tr>
<th>Step</th>
<th>Design and Implement WorkFlow</th>
<th>Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Learning Logic Circuit</td>
<td>TDeLS</td>
</tr>
<tr>
<td>2</td>
<td>Learning HDL</td>
<td>TDeLS</td>
</tr>
<tr>
<td>3</td>
<td>Learning Design of Circuit</td>
<td>TDeLS</td>
</tr>
<tr>
<td>4</td>
<td>Reuse &amp; Refer Resources of Circuits</td>
<td>TDeLS</td>
</tr>
<tr>
<td>5</td>
<td>Design Entry</td>
<td>Client</td>
</tr>
<tr>
<td>6</td>
<td>HDL Code Compiler</td>
<td>Client</td>
</tr>
<tr>
<td>7</td>
<td>Logic Synthesis</td>
<td>Client</td>
</tr>
<tr>
<td>8</td>
<td>Logic Simulation</td>
<td>Client</td>
</tr>
<tr>
<td>9</td>
<td>Placements and Routing</td>
<td>Client</td>
</tr>
<tr>
<td>10</td>
<td>Implementation to the actual target unit</td>
<td>Remote Lab.</td>
</tr>
<tr>
<td>11</td>
<td>Tests and Validations</td>
<td>Remote Lab.</td>
</tr>
<tr>
<td>12</td>
<td>Analysis of obtained data (post-analysis)</td>
<td>Client</td>
</tr>
</tbody>
</table>

**Top-down eLearning System (TDeLS)**: Top-down eLearning System (TDeLS). The TDeLS provides mechanisms for dynamic and efficient retrieval of suitable learning materials across the network such as the Internet. It assists the learner to achieve the learning goal efficiently. Using the TDeLS equipped with these mechanisms, learners can keep focusing on their primary interests to achieve their goals successfully [6]. From Step 1 to Step 4, in Table 1, TDeLS supports learners to study logic circuit design, HDL and circuit implementation.

**Remote Laboratory**: Recently, most learners own high-performance personal computers and have access to the Internet using the broadband connectivity from home. That leads us to organize them as integrated remote laboratory environment across the Internet. At Step 10 and 11 in Table 1, Remote Laboratory offer the services of experiment runs, circuit implementations, testing, obtaining measured data to analyze behaviors of circuits.

**Rich Client Site**: From Step 5 to Step 9, and Step 12 in Table 1, CPU intensive takes such as FPGA compilations be off-loaded from the server host and can be performed by each learner’s own client PC. Such a rich-client configuration allows the server to concentrate on the service management tasks and hardware resource managements.

**III. Hardware Logic Design**

At a modern logic design classroom, HDLs are mostly used to describe circuits for FPGAs. For designing the digital circuit on PC, the design process follows the sequence of function test, Design synthesis, and Timing simulation. Furthermore, the designed circuit can be actually implemented on FPGA/CPLD attached to the PC, and can be tested by running the hardware. These CAD tasks were usually performed by central servers in a time-sharing mode. Nowadays, PCs become powerful enough to perform such tasks locally decoupled from servers. So, each learner can design hardware.
independently. Thus the logic circuit design course is a suitable area to adopt the TDeLS.

- **Hardware Design Procedure**: This section describes the method of decomposing the circuit specification into a collection of modules. At first, the design specification of the circuit is given, and then it is decomposed into circuit modules, which implement separate functions. Next, each module is designed according to the specification. When there is a module which has already been designed, the module is reused and the circuit can be implemented without duplicating the design. Figure 3 shows the example of a circuit design flow. The target circuit is decomposed into two modules; module A and module B. The module A and B are further implemented separately and then combined to organize the desired circuit module.

![Figure 3](image)

**HARDWARE DESIGN PROCEDURE BY HDL.**

The HDLs allows us to employ the top-down design method. Figure 3 shows the design procedure based on the top-down design method. According to the specification of this target circuit, it is decomposed into two specification modules (Module A, B) which compose the target circuit. Then, Module A and B are further decomposed into the detailed modules. Finally, modules (module A1, A2, A3, B1, and B2) of these decomposed specifications are obtained.

- **Hardware Logic Design Contents**: As an example of the circuit design by making use of VerilogHDL, an 8bits CPU (Module name: TinyCPU) is employed for the final target circuit. Figure 4 shows the structure of the composition modules for this TinyCPU. The TinyCPU is composed of an arithmetic logic unit (ALU) controller and an xbitLatch. The module organization takes the form of a layered structure. The arithmetic logic unit consists of ALU={ADD, SUB, AND, OR, MUX}. Also, the xbitLatch can be composed in similar fashion.

![Figure 4](image)

**STRUCTURE OF MODULE FOR THE TINYCPU.**

- **eLearning Contents**: The learning contents for the target module are expressed in XML documents. The details of tags are described in Table 2. An attribute is added to compose the cellular models. Using this attribute, each module can be combined and the cell database is organized. Newly implemented circuit module can be added to the cell database via the Web.

<table>
<thead>
<tr>
<th>Tag Name</th>
<th>Meaning of Tag</th>
</tr>
</thead>
<tbody>
<tr>
<td>module_id</td>
<td>Unique ID of Module</td>
</tr>
<tr>
<td>module_profile</td>
<td>The profile of this module</td>
</tr>
<tr>
<td>module_spec</td>
<td>Outline specification of Module</td>
</tr>
<tr>
<td>generated_date</td>
<td>Date that this cell generated</td>
</tr>
<tr>
<td>Author</td>
<td>Author name</td>
</tr>
<tr>
<td>Module_name</td>
<td>Details of this VerilogHDL module</td>
</tr>
<tr>
<td>module_type</td>
<td>Indicate Target module or Simulation module</td>
</tr>
<tr>
<td>Port</td>
<td>Port Specification of Module</td>
</tr>
<tr>
<td>Signal</td>
<td>About the input-output port</td>
</tr>
<tr>
<td>name</td>
<td>Port name</td>
</tr>
<tr>
<td>direction</td>
<td>Input, Output, Inout</td>
</tr>
<tr>
<td>length</td>
<td>Bandwidth of Port</td>
</tr>
<tr>
<td>status</td>
<td>Kind of Signal (Bus, Control, Clock)</td>
</tr>
<tr>
<td>Sourcecode</td>
<td>HDL Source Code</td>
</tr>
<tr>
<td>Sentence</td>
<td>Source Code</td>
</tr>
</tbody>
</table>

- **The courseware generation algorithm**: Figure 5 shows the learning contents structure. The study route and a learning content cell structures are shown. The learning content is expressed in the form of a hierarchical order according to the learner’s skill level.

  The serialization [3] plays an important role in deciding and offering the order of the learning contents in the form of a learning sequence. For the serialization, three kinds of methods are employed to investigate the learning content cell structure and to decide the orders. The most suitable learning contents is recommended first, according to the learner’s current study order history. If it is not accepted, the second alternative is proposed, determined by the following serialization orderings.

  The eLearning system automatically generates the order of the learning material offering according to the serializing algorithm. The following three methods are employed as automatic serializations.

1. **The same dimension priority type**: The eLearning System pays attention to the dimension which is one of cell information. It offers a learning material which has the same dimension. From Figure 5, the dimensional order of cells is obtained as A4->B3->Z2->F2->Z1->F1->Y0->X0->M0. So, Serialized Order becomes as
2. The lower dimension priority type: The eLearning System offers a learning material which has the lower dimension than the current one. From Figure 5 the following two kinds of serialized orderings are obtained.

Ser1=<A4, B3, Z2, Z1, X0, Y0>
Ser2=<B3, F2, F1, M0>

The eLearning system composes these two serialized orders and generates the following a serialized order which implement the depth first algorithm.

Serialized Order
=<Ser1, Ser2>
=<A4, B3, Z2, Z1, X0, Y0, F2, F1, M0>

It is shown that Ser1 and Ser2 have derived from the B3 Cell in Figure 5. It is necessary to determine which cell should be selected for serialization. Proposed Top-down eLearning Tools uses learners information for the selection is decided according to learner's information.

3. Combination of the same and lower dimension priority types: This is a serialize method which uses the same dimension priority type together with the lower dimension priority type. The serialization strategy can be changed from the same priority to the lower priority, or vice versa, according to learners judges on the way to the goal. If the learner changes the strategy at F2 design stage, the serialization becomes the following order:

Serialized Order
=<A4, B3, Z2, F2, F1, M0, Z1, Y0, X0>

IV. Hardware Experiment Environment

To realize the remote laboratory features using these networking environments, we should consider the following features: 1) Multi-User Support, 2) Job Management, 3) Service Registry, and 4) Experiment Platform Allocations. The overview of the proposed architecture of multi-user remote laboratory system, which implements these features, is shown in the Figure 6.

- **Multi-User Support**: Existing other remote laboratories usually limit the number of users to the number of actual available resources [11]. Because, these systems are simply client-server systems [12] and the scheduler for processing user requests are not fully functional to support the multi-user time-sharing system. The combinatorial use of FPGA/PC and PC-based measurement tools has made it possible to develop a remote multi-user time-sharing hardware experiment system, where learners can perform actual experiments using actual hardware equipments and tools concurrently. The distributed remote laboratory system can deliver higher efficiency in multi-user environments.

- **Job Management System**: The multi-user remote laboratory has the ability of Job Management and Distributed Resources Management. It resolves conflicts among users, when many users request the same services at the same time. Job management prevents contentions and arranges the service scheduling.

- **Service registry**: The service registry specifications define a way to discover the Experiment Platform. The specification consists of target related documents, such as the platform ID, the IP address, the supported target devices, the measurement equipments and so on. It provides a mechanism for users to dynamically find out the Experiment Platforms necessary to carry out specific experiments.

- **Experiment Platform**: The experiment platform (Figure 7) implemented in this new Remote Laboratory Environments is built on PC based measurement equipments such as a Logic Analyzer/Pattern Generator, target unit with FPGA and the experiment server to manage these equipments. Its major roles are: to allocate measurement/target unit equipment resources and to control the job executions, which are designated by the Condor job allocation system.

EVALUATIONS

Table 3 shows the waiting-time results in the multi-user/single-platform environment, ten user(s) request to
running experiments simultaneously. The resulting waiting-time consists of the following five parts: waiting-time before starting experiment, setup-time for measurement conditions, FPGA programming-time to load a circuit data, measurement time, and reply-time to return results. The average measurement time of each user is set around 48 seconds. The resulting waiting-time in Table 3 increase almost linearly according to the waiting queue length. At most ten pending users are waiting for the same services simultaneously. These results show that there are not any conflicts among users, and the job manager worked properly with minimum overhead.

### TABLE 3

<table>
<thead>
<tr>
<th>User(s)</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
</tr>
</thead>
<tbody>
<tr>
<td>Waiting Time (sec)</td>
<td>57</td>
<td>112</td>
<td>167</td>
<td>221</td>
<td>277</td>
<td>331</td>
<td>387</td>
<td>441</td>
<td>496</td>
<td>551</td>
</tr>
</tbody>
</table>

### CONCLUSIONS

It has shown that the selection of the learning materials is effective by employing the top-down method for hardware logic circuit design course. The remote laboratory for logic circuit design by making use of VerilogHDL has been carried out. It is shown that preparing the learning materials packed with XML and providing the learners with these materials via the Web/Internet, made the courseware easy to implement and effective. One of the successful ideas obtained through the development of the system is its generic use of job management organizations. It achieved effective and practical operations of a remote multi-user time-sharing hardware experiment system.

The advantages applying the new remote laboratory are: 1) Location-free efficient sharing of actual experiment equipments. 2) Cost-effective way of sharing expensive measurement equipments. 3) Get the feeling of handling actual measurement equipments and hardware from the remote site. 4) Remote acquisition of actual measured data to analyze the designed digital circuits.

This integrated system allows learners to come and go between actual laboratory and new remote laboratory in a seamless way, and to shorten the entire design cycle.

### REFERENCES


